REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application. The Examiner additionally stated that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are rejected. By this amendment, claims 1, 11, and 21 are amended. Hence, claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1, 11, and 21 under 35 U.S.C. 103(a) as being unpatentable over the background of the specification in view of Philip, U.S. Patent No. 3,130,387 (hereinafter, "Philip"). Applicant respectfully traverses the Examiner's rejections.

The Examiner noted that the background of the instant application specification teaches a microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

- a translator, configured to generate a plurality of micro instructions corresponding to an instruction and a microcode entry point (Spec: 0007); and
- early access logic, couple to said translator, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic, and wherein said translator provides said plurality of micro instructions to said register logic (Spec: 0009) (The Examiner stated that all of this inherently flows from the specification and that it would be inefficient to have another unit generate the ROM address when the translator is already determining what the instruction is.)

The Examiner stipulated that the only aspect that is not taught by the specification is a buffer between the translator and the register logic and that the inventors have identified the problem that exists in the dual translation process described in 0009 of the specification is that the translator and the ROM can get out of synchronization because of delay caused by a larger ROM. The Examiner opined that the problem described is a very old one that has been resolved long ago (Philip: Title), and that one of ordinary skill in the pertinent art would have readily realized that when two independent data producing objects become unsynchronized, that a buffer may be implemented.

The Examiner rejected claims 11 and 21 for the same reasons.

In reply, Applicant respectfully directs the Examiner's attention to the background of the specification, paragraph [0009], which is repeated below for ease of reference.

> **[0009]** For this reason, it is not uncommon in the art to find that a combination of the above two techniques is employed to translate instructions into corresponding micro instruction sequences. For instance, direct translation is often provided to translate those instructions having micro instruction sequences consisting of number of micro instructions that can be directly translated within the delay that would be otherwise experienced by providing those instructions to a microcode ROM. And for those instructions that have a corresponding number of micro instructions that are greater than what could be generated during the microcode ROM access delay time, an address is provided to the microcode ROM for a second part of a corresponding micro instruction sequence while at the same time a first part of the micro instruction sequence is directly translated. Consequently, during the clock cycle following when the last instruction of the first part of the micro instruction sequence is directly generated, a first instruction from the second part of the micro instruction sequence is provided by the microcode ROM. In this manner, the access delay of the microcode ROM is effectively absorbed by direct translation and instruction translation efficiency of an associated microprocessor is maximized.

Applicant respectfully asserts that nowhere within the above paragraph, no anywhere else within the background section of the specification does Applicant teach early access logic, coupled to said translator, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic. This paragraph and the background do not teach early access logic because it is assumed that both the translator and microcode ROM are in synchronization, in other words, as is taught in an excerpt from paragraph [0026] of the specification, which expands upon the background:

> When an entry from the micro instruction queue 112 is provided to the register stage 103, its microcode entry point is provided to the microcode ROM 111 via the access bus 113. If no micro instructions are provided in the entry by the translator 110, then the register stage inserts slips (also called "holes," "stalls," or "voids") into the pipeline of the microprocessor 100 in synchronization with a pipeline clock signal (not shown) until the microcode ROM 111 begins providing micro instructions corresponding to the microcode entry point provided over bus 113.

Yet, the background clearly teaches a problem that has been observed by the present inventors due to mismatched translator and microcode ROM delay, as is detailed in paragraphs [0010] – [0012]:

> **[0010]** As alluded to above, changes to sequence of micro instructions that implement certain ISA-level instructions can be easily made to a design that employs microcode ROM lookup, or a combination of direct translation and microcode ROM lookup, for translation. Nevertheless, the present inventors have observed that there are cases where the attributes (e.g., overall capacity or entry size) of a given microcode ROM are insufficient to implement changes. In such cases, it is necessary to replace the microcode ROM with one whose attributes support the changes. Often these changes require greater capacity or entry size, and a ROM that provides these greater attributes typically exhibits a greater access delay.

> **[0011]** So, the problem that the present inventors note is one in which a new microcode ROM presenting a greater delay is required to interoperate efficiently with existing direct translation logic. The direct translation logic is configured to generate a first part of a sequence of micro instructions during the access delay time of the former microcode ROM and, as a result, interoperation with the new microcode ROM results in slips or voids in a microprocessor pipeline between the time that the direct translation logic finishes generation of the first part of the sequence and the time when the new microcode ROM begins providing a second part of the sequence.
>
> **[0011]** Therefore, what is needed is a microprocessor apparatus that precludes pipeline stalls during instruction translation which are due to microcode ROM access delay.

In view of the above points, Applicant respectfully asserts that the background of the specification clearly fails to teach early access logic, coupled to said translator, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic. Rather, the background is silent with respect to early access logic, and paragraph [0026] of the specification further specifies that the microcode ROM is accessed, not prior to providing the microcode entry point to register logic, but when it is provided to register logic.

With regard to the Examiner's assertion that the only aspect that is not taught by the specification is a buffer between the translator and the register logic and that the inventors have identified the problem that exists in the dual translation process described in 0009 of the specification is that the translator and the ROM can get out of synchronization because of delay caused by a larger ROM, Applicant respectfully disagrees, and asserts that the aspect not taught by the background is the early access logic, not the buffer, and that it is the early access logic that is required to access the buffer prior to when a micro instruction queue entry is provided to register logic in a following stage.

Applicant has shown that the background of the specification does not teach early access logic, and the buffer taught by Philip does not suggest, or provide any other motivation to one skilled for the provision of early access logic. Consequently, it is requested that the rejection of claims 1, 11, and 20 be withdrawn.

The Examiner also rejected claims 1, 3-5, 8-11, 13-15 and 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carbine et al. (US Patent 5,222,244) (hereinafter, "Carbine), in view of the background of the specification. Applicant respectfully traverses the rejections.

Applicant notes that claim 26 was cancelled in a previous communication, thereby rendering the rejection moot.

As per claim 1, the Examiner noted that Carbine teaches a microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

- a plurality of micro instruction queue entries, each corresponding to an instruction, and said each comprising a plurality of micro instructions and a microcode entry point (column 6, lines 58-68; column 7, lines 1-19); and
- early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic (column 8, lines 39-46).

The Examiner stated that Carbine does not teach the microprocessor apparatus comprising:

- a translator, coupled to said plurality of micro instruction queue entries, configured to generate said microcode instruction queue entry (column 6, lines 58-68; column 7, lines 1-19);

and that Carbine does not disclose how the contents of the queue entries are determined, but that Applicant has disclosed as prior art that the combination of a microcode ROM and a direct translator for the sequencing of macroinstructions is known in the art.

The Examiner noted that the combination of the microcode ROM and a direct translator in coordination with the microcode queue would be a viable, beneficial solution in Carbine, and further pointed out that an opposing possibility would be to statically populate the queue with the most commonly used instructions. The Examiner stated that one of ordinary skill in the pertinent art would have recognized that this would not be extremely useful because it would only provide the benefits of not stalling on a microcode ROM instruction in the instance of encountering a common instruction, which might not extend across different applications, and that, in contrast, a queue that is dynamically populated by a translator when the microcode ROM instruction is first encountered will provide the benefits of the invention to all microcode ROM instructions. The Examiner thus concluded that it would have been obvious to one of ordinary skill in the pertinent art at the time of the invention that providing a translator to generate the microinstruction queue entries in Carbine would provide the benefit of not stalling on any microcode ROM instruction, rather than a select few, and that it is inherent that that translator will generate the micro instruction queue entries in order, since the translate requests would be sent to it in order and the register logic would need the entry in order. The Examiner inferred from this that it is inherent that the queue will receive the entries in order and will deliver them in order and that what cannot be inferred by this combination, however, is that said early access logic employs said microcode entry point when it is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle. The Examiner noted that this is because there is no evidence that Carbine's microcode translation ROM is a FIFO queue and that the combination suggested could very well just put the next entry in the first available slot. However, the Examiner pointed out since it has been established that the entries would have to be provided to the register logic in the order that they were created, this would mean that each entry would need a tag associated

with it, numbered to correspond to when it was entered into the queue, and that one of ordinary skill in the pertinent art however will realize that this creates some obstacles. The Examiner further noted that comparing tags in any unstructured (i.e. randomly ordered) storage area is time consuming, and that the extra field required to mark all of the entries also uses up space and wastes power, but on the other hand, keeping the entries in order means only having to check one register to see where the head of the queue is quick and easy. Consequently, the Examiner concluded that one of ordinary skill in the pertinent art would be motivated to use a structured FIFO queue rather than a random queue.

Applicant respectfully disagrees with the Examiner's characterization of the teachings of Carbine and of the background of the specification and offers the following arguments in traversal. First, claim 1, as amended herein, is provided below for ease of reference.

1. A microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

a translator, configured to generate a plurality of micro instruction queue entries, each of said plurality of micro instruction queue entries corresponding to an instruction, and said each of said plurality of micro instruction queue entries comprising a plurality of micro instructions and a microcode entry point, wherein said translator generates said each of said plurality of micro instruction queue entries in order;

a micro instruction queue, coupled to said translator, configured to receive said each of said plurality of micro instruction queue entries in said order, and configured to provide said each of said plurality of micro instruction queue entries to register logic in said order;

a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point; and

> early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access said microcode ROM prior to when said microcode entry point is provided to said register logic, whereby said microcode ROM provides a first micro instruction from said second part to said register logic when said first micro instruction is required by said register logic, and wherein said early access logic employs said microcode entry point when said microcode entry point is within a bottom micro instruction queue entry, said bottom micro instruction queue entry comprising one of said each of said plurality of micro instruction queue entries, and wherein said bottom micro instruction queue entry will be provided to said register logic during a next clock cycle.

Note that claim 1, in combination with other elements and limitations, recites both a translator and a microcode ROM. Clearly, the background teaches these elements. But neither Carbine nor the background teach in combination:

- a microcode ROM, configured to provide a second part of a micro instruction sequence corresponding to said microcode entry point; and
- early access logic, coupled to said micro instruction queue, configured to employ said microcode entry point to access said microcode ROM prior to when said microcode entry point is provided to said register logic

Applicant respectfully submits that the section of Carbine which the Examiner relies upon to teach "early access logic . . . to access said microcode ROM" (column 8, lines 39-46) is misunderstood by the Examiner. Note in this section (and many other areas of Carbine) that he refers to a "translation ROM (122). Within the noted section he states, "the translation ROM contains not only the instructions, but it also contains the address in the microcode ROM to fetch the rest of the instructions from." Clearly, the "translation ROM" (122) is not equivalent to the microcode ROM of claim 1. It is, rather, similar to the translator element. Carbine also teaches that the microcode ROM (not the translation ROM) is part of the instruction fetch unit (50) shown in FIG. 2 and described more fully in copending application Ser. No. 07/630,498. (col. 8, lines 15-18) Thus, the elements of

Carbine (i.e., microflow word multiplexer logic (112) that looks ahead in order to set-up inputs to the translation ROM (122)) that the Examiner relies upon to teach the early access logic of claim 1 are without a doubt not coupled to a microcode ROM, but rather to a translator. Carbine addresses an entirely different problem than is addressed by the present invention.

Accordingly, in view of the arguments submitted above, Applicant requests that the rejection of claim 1 be withdrawn.

Claims 3-5 depend from claim 1 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

Claim 11 recites substantially the same elements as have been argued above as being allowable over the noted references. Therefore, Applicant respectfully requests that the rejection of claim 11 be withdrawn as well.

Claims 13-15 and 17-20 depend from claim 11 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

Claim 21 recites substantially the same elements as have been argued above as being allowable over the noted references. Therefore, Applicant respectfully requests that the rejection of claim 21 be withdrawn as well.

Claims 22-25 and 27-29 depend from claim 21 and add further limitations over that which has been argued as being allowable over the noted references and it is accordingly requested that the rejections be withdrawn.

In reply to the Examiner's assertion that Carbine's translation ROM is not equivalent to Applicant's translator because the translator is a direct translation unit as addressed in paragraph 2 of section 48 of the disclosure and, on the other hand, Carbine's translation ROM is a lookup translation unit, Applicant respectfully asserts that *how* the direct translation is performed is not relevant to this disclosure. What is relevant is that a translator receives instructions and outputs both micro instructions and a microcode entry

point. This description applies to both Carbine's translation ROM and to applicant's translator. Furthermore, the description of applicant's microcode ROM and Carbine's microcode ROM (part of the instruction fetch unit (50)) match in the sense that they both accept an address from which to fetch remaining micro instructions.

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CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By: _____

RICHARD K. HUFFMAN, P.E.
Registration No. 41,082
Tel: (719) 575-9998

01/17/2007

Date: _____